Table 14. PLL, Clocking, Watchdog, and Low-Power Mode Registers (continued)

Name	Address	Size (x16)	Description
PCLKCR3	0x0000-7020	1	Peripheral Clock Control Register 3
PLLCR	0x0000-7021	1	PLL Control Register
SCSR	0x0000-7022	1	System Control and Status Register
WDCNTR	0x0000-7023	1	Watchdog Counter Register
WDKEY	0x0000-7025	1	Watchdog Reset Key Register
WDCR	0x0000-7029	1	Watchdog Control Register
BORCFG	0x000985	1	BOR Configuration Register

3.1.1 Enabling/Disabling Clocks to the Peripheral Modules

The PCLKCR0/1/3 registers enable/disable clocks to the various peripheral modules. There is a 2-SYSCLKOUT cycle delay from when a write to the PCLKCR0/1/3 registers occurs to when the action is valid. This delay must be taken into account before attempting to access the peripheral configuration registers. Due to the peripheral-GPIO multiplexing at the pin level, all peripherals cannot be used at the same time. While it is possible to turn on the clocks to all the peripherals at the same time, such a configuration may not be useful. If this is done, the current drawn will be more than required. To avoid this, only enable the clocks required by the application.

Figure 14. Peripheral Clock Control 0 Register (PCLKCR0)

15	11	10	9	8
Reserved		SCIAENCLK	Reserved	SPIAENCLK
R-0		R/W-0	R-0	R/W-0

7	5	4	3	2	1	0
Reserved		I2CAENCLK	ADCENCLK	TBCLKSYNC	Reserved	HRPWMENCLK
R-0		R/W-0	R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. Peripheral Clock Control 0 Register (PCLKCR0) Field Descriptions

Bit	Field	Value	Description
15-11	Reserved		Any writes to these bit(s) must always have a value of 0.
10	SCIAENCLK		SCI-A clock enable
		0	The SCI-A module is not clocked. (default) (1)
		1	The SCI-A module is clocked by the low-speed clock (LSPCLK).
9	Reserved		Any writes to these bit(s) must always have a value of 0.
8	SPIAENCLK		SPI-A clock enable
		0	The SPI-A module is not clocked. (default) (1)
		1	The SPI-A module is clocked by the low-speed clock (LSPCLK).
7-5	Reserved		Any writes to these bit(s) must always have a value of 0.
4	I2CAENCLK		I^2C clock enable
		0	The I^2C module is not clocked. (default)(1)
		1	The I^2C module is clocked.
3	ADCENCLK		ADC clock enable
		0	The ADC is not clocked. (default) (1)
		1	The ADC module is clocked

(1) If a peripheral block is not used, the clock to that peripheral can be turned off to minimize power consumption.